CLAIMS

I CLAIM:

1. A decoder for a communication system, the decoder comprising:

a first decoder block that receives a soft-input information bit for decoding and calculates a probability estimate for the soft-input information bit;

a second decoder block configured to receive and process the probability estimate of the soft-input information bit using modulo arithmetic operations; and

a decision module adapted to receive the processed soft-input information bit and to generate hard-decision output information.

2. A decoder as defined in claim 1, wherein the first decoder block includes an output element configured to receive the soft-input information bit and to generate extrinsic information.

3. A decoder as defined in claim 2, further comprising:

an interleaver configured to interleave the received output extrinsic information, and to direct the interleaved output to the second decoder block.

4. A decoder as defined in claim 3, wherein the second decoder block includes a state metric calculator configured to calculate backward and forward metrics using the soft-input information bit and the extrinsic information.

5. A decoder as defined in claim 4, further comprising:

a deinterleaver configured to deinterleave output of the second decoder block, and to feed the deinterleaved output back to the first decoder block.

6. A decoder for a communication system, the decoder comprising:

an iterative decoding module configured to receive soft-input information bits, the iterative decoding module iterating on probability estimates of the soft-input information bits to generate soft-decision output information, wherein the iterative decoding module generates and processes both backward and forward metrics substantially simultaneously using modulo arithmetic operations; and

an output module configured to receive the soft-decision output information and to generate hard-decision output information.

7. A decoder as defined in claim 6, wherein the iterative decoding module includes two sub-modules to simultaneously process first and second stages of trellis decoding.

8. A decoder as defined in claim 7, wherein the iterative decoding module includes an output element configured to receive the soft-input information bits and output extrinsic information on the first and second stage of trellis decoding.

9. A decoder as defined in claim 8, further comprising:

an interleaver configured to interleave the received output extrinsic information, and to direct the interleaved output to the iterative decoding module for the second stage of trellis decoding.

10. A decoder as defined in claim 8, further comprising:

a deinterleaver configured to deinterleave the received output extrinsic information, and to direct the deinterleaved output to the iterative decoding module for the first stage of trellis decoding.

11. A module as defined in claim 6, wherein the iterative decoding module is a maximum a priori (MAP) decoder.

12. A receiver for a communication system, comprising:

an RF unit configured to receive RF signals and to down-convert the signal to a baseband signal;

a demodulator configured to demodulate, process, and digitize the baseband signal into soft-input information bits; and

an iterative decoding module configured to receive the soft-input information bits, the iterative decoding module iterating on probability estimates of the soft-input information bits to generate hard-decision output information, wherein the iterative decoding module includes a plurality of arithmetic modules operating to generate and process both backward and forward metrics substantially simultaneously using modulo arithmetic operations.

13. A receiver as defined in claim 12, wherein the demodulator includes a demapper for converting the digitized data into the soft-input information bits.

14. A receiver as defined in claim 12, wherein the demodulator is a multicarrier demodulator.

15. A receiver as defined in claim 14, wherein the multicarrier demodulator includes a fast Fourier transform module to calculate Fourier transforms of the baseband signals.

16. A receiver as defined in claim 12, wherein the plurality of arithmetic modules includes two sub-modules to simultaneously process first and second stages of trellis decoding.

17. A soft-input soft-output (SISO) decoding block for a communication system, the block comprising:

a first plurality of modules configured to receive soft-input backward state metrics, the first plurality of modules operating to process the backward state metrics using modulo arithmetic;

a first multiplexer to select the backward state metrics;

a second plurality of modules configured to receive soft-input forward state metrics, the second plurality of modules operating to process the forward state metrics using modulo arithmetic; and

a second multiplexer to select the forward state metrics.

18. A block as defined in claim 17, wherein the SISO block is a maximum a priori (MAP) decoder.

19. A block as defined in claim 17, wherein the first plurality of modules includes a first modulo arithmetic comparator to provide a selection signal to the first multiplexer.

20. A block as defined in claim 17, wherein the second plurality of modules includes a second modulo arithmetic comparator to provide a selection signal to the second multiplexer.

21. A block as defined in claim 17, further comprising:

a third multiplexer configured to provide an appropriate branch metrics for the first and second plurality of modules.

22. A block as defined in claim 21, further comprising:

an input clock configured to synchronize and control processing of the backward and forward state metrics.

23. A block as defined in claim 21, wherein the third multiplexer includes a first signal element to enable the first plurality of modules at rising edges of the input clock.

24. A block as defined in claim 22, wherein the third multiplexer includes a second signal element to enable the second plurality of modules at falling edges of the input clock.

25. A method of decoding soft-input symbol block data in a communication system, comprising:

performing backward recursion of a trellis diagram by computing backward state metrics of each node on the trellis diagram of the symbol block data;

storing the backward state metrics to a storage mechanism;

performing forward recursion of the trellis diagram by computing forward state metrics of each node on the trellis diagram of the symbol block data; and

calculating extrinsic information.

26. A method as defined in claim 25, further comprising:

computing first and second branch metrics along branches from two previous nodes of the trellis diagram.

27. A method as defined in claim 26, wherein performing backward recursion on a trellis diagram includes computing a sum comprising a previous backward state metric multiplied by a first branch metric and a previous backward state metric multiplied by a second branch metric.

28. A method as defined in claim 26, wherein calculating extrinsic information includes computing a log likelihood ratio for each time point of the trellis diagram.

29. A method as defined in claim 26, wherein computing a log likelihood ratio includes:

detecting when a decoded bit is determined to be a '1'; and

computing a first sum of a plurality of products of the backward state metrics, forward state metrics, and the first and second branch metrics at a particular time that is associated with a decoded bit representation '1'.

30. A method as defined in claim 29, wherein computing a log likelihood ratio includes:

detecting when a decoded bit is determined to be a '0'; and

computing a second sum of a plurality of products of the backward state metrics, forward state metrics, and the first and second branch metrics at a particular time that is associated with a decoded bit representation '0'.

31. A method as defined in claim 30, wherein computing a log likelihood ratio includes dividing the first sum by the second sum.

32. A method as defined in claim 31, wherein calculating extrinsic information includes subtracting a probability estimate of the soft-input symbol block data from the log likelihood ratio.

33. A method as defined in claim 32, further comprising:

iterating on performing backward recursion, storing, performing forward recursion, and calculating extrinsic information.

34. A method as defined in claim 33, further comprising:

retrieving decoded information bits from the iterating by examining a sign bit of the log likelihood ratio.

35. A method as defined in claim 34, further comprising:

outputting a hard-decision bit as a '1' if the sign bit is positive; and

outputting a hard-decision bit as a '0' if the sign bit is negative.

36. A method as defined in claim 25, further comprising:

dividing the symbol block data into a plurality of windows, each window including soft-input bits.

37. A method as defined in claim 36, wherein dividing the symbol block data includes allowing overlaps between the plurality of windows.

38. A method as defined in claim 36, further comprising:

processing the soft-input bits of the plurality of windows in parallel.

39. A method as defined in claim 38, further comprising:

interleaving the soft-input bits in the plurality of windows.